Code No. BTS 004 (B)

B.TECH. DEGREE III SEMESTER EXAMINATION IN COMPUTER SCIENCE AND ENGINEERING/ ELECTRONICS AND COMMUNICATION ENGINEERING/ ELECTRONICS AND BIOMEDICAL ENGINEERING/ELECTRONICS AND INSTRUMENTATION ENGINEERING JANUARY 2001

CS/EC/EB/EI 304 DIGITAL ELECTRONICS

Time: 3 Hours Maximum Marks: 100

UNIT - I

I. (a) Perform the following arithmetic operations. (5)

(i) $136.02_8 \times 2.4_8$ (ii) $231.06 + 1.3_8$

(b) Double precision floating point numeric data uses 53 bits for mantissa that includes a sign bit are used for biased exponent. Calculate the maximum number of decimal digits that can be stored by this representation and the maximum and minimum values of the exponential taking proper constant as bias. (5)

(c) Design a BCD to Decimal decoder. Simplify the output using K-map. Draw the logic diagram. (10)

OR

II. (a) Perform the following operations using signed 1's and 2's complement representation. (5)

(i) (+73) + (-14) (ii) (-73) - (-14)

(b) Explain how addition and subtraction can be performed in XS3 codes. (5)

(c) Find a minimal cover for the function given

$G(A, B, C, D, E) = \Sigma (0, 1, 2, 3, 4, 6, 8, 11, 12, 27, 28) + \Sigma_d (9, 16, 17, 18, 19)$ (10)

UNIT - II

III. (a) Draw the logic circuit for a 4 stage Register with parallel transfer of input data and shift right output data using JK flipflop and explain the operation. (10)

(b) Design a logic sequence detector which recognizes 4 consecutive 1's. Draw the logic diagram. (10)

OR

IV. (a) Construct a 4 bit ripple counter and explain. Also explain the operation of JK Master Slave flipflop using truth table and logic diagram. (10)

(b) Design a counter using RS flipflop to count the sequence given

ABC = 000, 111, 101, 110, 001, 010 and repeat. (10)

UNIT - III

V. (a) Design a 4 bit combinational decrementer using full adder circuit. (10)

(b) Construct a circuit to add two 4 bit numbers and explain. Use half adder and other gates. (10)

OR

VI. (a) Design a full subtractor using NOR gates only. (10)

(b) Explain the operation of

(i) Astable Multivibrator (ii) Bistable Multivibrator using 555 Timer. (10)

(Turn over)

UNIT - IV

VII. (a) Represent the tree structure of memory hierarchy in a computer system and explain each component of the same. (10)

(b) Draw the circuit for a typical CAM memory cell. Explain how Read and Write operations are carried out. (10)

OR

VIII. (a) Draw the circuit for a typical semiconductor memory cell. Explain how Read and Write operations are carried out. (10)

(b) Explain the concept of Virtual memory and Cache memory. (10)

UNIT - V

IX. (a) Explain with circuit diagram a typical TTL NOR gate with totem pole output. (10)

(b) Write short notes on the following:

(i) Propagation delay
(ii) fan in
(iii) fan out
(iv) Noise Margin (10)

OR

X. (a) Describe about fanin fanout of standard CMOS devices. Compare CMOS with TTL. (10)

(b) Describe with diagram the interfacing of CMOS to TTL. (10)

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