

**B.Tech. Degree III Semester (Special Supplementary) Examination  
September 2004**

**CS/EC/EB/EI/EE 304 DIGITAL ELECTRONICS**

(2002 Admissions)

Time: 3 Hours

Maximum Marks: 100

- I. (a) (i) Convert the binary number 11011110 into its decimal equivalent. (6)  
 (ii) Add 956 and 492 in 8421 BCD code. (6)  
 (b) (i) Convert  $7325_{16}$  to its decimal equivalent. (6)  
 (ii) Convert decimal 62 to XSZ form. (6)  
 (c) (i) How will you assemble an inverter by using a NAND gate or a NOR gate?  
 (ii) Sketch a circuit to implement the equation given below: (8)  

$$X = A \cdot B + C \cdot D$$
- OR**
- II. (a) (i) Explain what is a multiplexer and demultiplexer. (8)  
 (ii) What are the two main categories of logic circuits? Explain. (8)  
 (b) Simplify the following function: (6)  

$$F = A \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C} + \bar{A} \cdot B \cdot C$$
  
 (c) Plot the following Boolean function on a map. (6)  

$$F = \sum(0,3,4,5,6,8,10,12)$$
- III. (a) How will you connect a JK flipflop so that it function as a clocked D latch? (6)  
 (b) What are asynchronous and synchronous counters? (4)  
 (c) With suitable diagrams and waveforms explain a four stage Johnson counter. (10)
- OR**
- IV. (a) What are flip flops? (4)  
 (b) Explain with truth table and diagrams an RS NAND latch and NOR latch. (6)  
 (c) How many JK flip flops will you require to make the following modulo counters? Explain with diagram. (10)  
 (i) mod - 4 (ii) mod - 6 (iii) mod - 9 (iv) mod - 11
- V. (a) Show the multiplication of binary number 10101 by 11010. (4)  
 (b) Explain with diagram the configuration of a 4 bit parallel adder. (8)  
 (c) Calculate the frequency and duty cycle of the output of an astable multivibrator using timer 555. Data given are  $R_A = 27K \text{ ohm}$   $R_B = 56K \text{ ohm}$   $C = 0.01 \mu\text{F}$ . (8)
- OR**
- VI. (a) Explain with waveform how a monostable multivibrator can be used as a pulse shaper. (8)  
 (b) Explain with neat diagram a serial adder. (8)  
 (c) Draw the Logic symbol and truth table of a half subtractor. (4)
- VII. (a) What is a Random Access Memory? Explain static RAM with a block diagram. Give the diagram and explain the serial expansion of memory cells to function as a  $4 \times 1$  RAM. (15)  
 (b) Explain what is meant by PAL and PLA. (5)
- OR**
- VIII. (a) What are the differences between static and dynamic RAM? Give the diagram of a basic DRAM memory cell. Explain. (10)  
 (b) With logic symbol diagrams, show how will you connect 2, 4116 DRAM ICs to build a  $16 K \times 2$  bit memory. (10)
- IX. (a) Explain briefly the classification of Logic families. (6)  
 (b) Give the three-state output configuration for a NAND gate. Write the truth table. Mention the application of three-state devices. (8)  
 (c) Explain the interfacing of CMOS to TTL. (6)
- OR**
- (a) Give the specifications and characteristics of basic TTL circuits. (8)  
 (b) Explain the following terms connected with TTL devices. (12)  
 (i) Fan-in and Fan-out (ii) Noise Margin  
 (iii) Propagation delay (iv) Speed-power relation

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