

B. Tech Degree III Semester Examination, November 2005**CS/EC/EB/EI/EE 304 DIGITAL ELECTRONICS***(Prior to 2002 Admissions)*

Time : 3 Hours

Maximum Marks : 100

- I. (a) Convert the following hex number to its equivalent (DAD) 16 :
 (i) Octal number (ii) BCD
 (iii) Decimal (iv) Excess 3
 (v) Binary. (5)
- (b) (i) Minimize the given Boolean function using K map.

$$F = \sum m(1, 3, 4, 6, 9, 11) + d(12, 14)$$
(A, B, C, D) (10)
 (ii) Implement the ckt using 2i/p NAND gates. (5)
- OR**
- II. (a) Minimize the given function using Queme-Mcbesky method :

$$F = \sum m(5, 7, 13, 15) + d(0, 2, 8, 10)$$
(A, B, C, D) (10)
 (b) Differentiate between (i) decoder and encoder (ii) multiplexer and demultiplexer. (10)
- III. (a) Draw the NAND implementation of a JK flip flop and explain. (10)
 (b) Design a sequence generator which generates the sequence 0-1-3-2 → using T flip flops. (10)
- OR**
- IV. (a) What is race around condition? How can it be avoided? (8)
 (b) Compare and contrast –
 (i) Asynchronous and synchronous counters
 (ii) Ring counter and Johnson counter
 (iii) Sequential circuit and combinational circuit. (12)
- V. (a) Draw the circuit of a serial adder and explain. (10)
 (b) With the help of necessary waveforms explain an astable multivibrator using gates. (10)
- OR**
- VI. (a) Design a full adder using gates. (8)
 (b) Draw the circuit for binary multiplication and explain. (12)
- VII. (a) Differentiate between (i) PAL and PLA (ii) ROM and RAM. (10)
 (b) Implement the following Boolean functions using PLA :
 (i) $F_1(A, B, C) = \sum m(0, 1, 5, 7)$
 (ii) $F_2(A, B, C) = \sum m(2, 4, 5, 6)$ (10)
- OR**
- VIII. (a) Draw the circuit of a static MOS memory cell and explain. (10)
 (b) Why is refreshing required in dynamic memory? (5)
 (c) What is PLD? (5)
- IX. (a) Draw the circuit of a TTL inverter and explain the transfer characteristics. (15)
 (b) Define fan in and fan out. (5)
- OR**
- X. (a) Define the following terms :
 (i) Noise margin (ii) Propagation delay. (8)
 (b) Explain how a standard TTL can be interfaced with CMOS gate. (12)

