

**B.Tech. Degree III Semester Examination, November 2004****CS/EC/EB/EI/EE 304 DIGITAL ELECTRONICS**

(2002 Admissions onwards)

Time: 3 Hours

Maximum Marks: 100

- I. (a) (i) Multiply the binary number 1101 by 1010. (6)  
 (ii) Divide 1011010 by 110. (6)  
 (b) (i) Convert the hexadecimal number CF3D to its decimal equivalent. (6)  
 (ii) Convert binary number 11011.101 to BCD form. (6)  
 (c) (i) Simply the following function:  

$$F = C(B + C)(A + B + C)$$
  
 (ii) Explain De Morgan's theorem. (8)
- OR**
- II. (a) Draw a Karnaugh map to represent the following, Boolean expression  

$$F = \overline{A}\overline{B}\overline{C}D + ACD + B\overline{D} + AB + BC$$
 (6)  
 (b) Realise all the basic gates using NAND and NOR gates. (10)  
 (c) Subtract using 2's complement method:  
 (i)  $4A6B_{(H)} - 30BC_{(H)}$   
 (ii)  $5237_{(H)} - 4F18_{(H)}$  (4)
- III. (a) Explain briefly the J - K Master-Slave Flipflop. (6)  
 (b) Explain with suitable diagrams and waveforms an edge triggered D flipflop. (6)  
 (c) Explain with relevant logic diagram, truth table and waveforms a MOD - 5 asynchronous counter. (8)
- OR**
- IV. (a) Explain with diagram and truth table the conversion of JK flipflop to SR flipflop and D flipflop. (7)  
 (b) Explain with waveforms a 4 bit binary ripple up counter. (7)  
 (c) Explain a JK flip flop shift register. (6)
- V. (a) Draw the logic diagram of a full adder. Explain the operation with a truth table. (8)  
 (b) Multiply 1110 by 1010. (4)  
 (c) Explain with Logic symbol and waveform a monostable multivibrator. Draw the diagram of a monostable multivibrator using discrete components. (8)
- OR**
- VI. (a) Draw and explain the circuit diagram of half adder using only NAND gates. (8)  
 (b) What is an ALU? (4)  
 (c) Explain any four applications of monostable multivibrators. (8)
- VII. (a) Give the different classification of memories. (8)  
 (b) Explain the serial-parallel expansion of memories. Give the diagram of serial-parallel expansion of memory cells to function as a 4 x 4 RAM using 1 x 4 RAMs. (12)
- OR**
- VIII. (a) Give the pin connections for IC 2114. Explain with circuit diagram, how two ICs 2114 connected to form a 2K byte x 4 bit memory. (10)  
 (b) What are programmable logic arrays? Explain. (5)  
 (c) Explain what is meant by Flash memory? (5)
- IX. (a) With a circuit diagram explain a typical TTL NAND gate. (8)  
 (b) Write short notes on the following terms connected with TTL devices:  
 (i) Propagation delay (ii) fan in and fan out  
 (iii) Noise margin (iv) Speed - power relation (12)
- OR**
- X. (a) Give and explain the classification of logic families. (5)  
 (b) What are three state devices? Explain. (5)  
 (c) Explain the interfacing of TTL to CMOS. (10)

