

B.Tech Degree III Semester Examination November 2002

CS/EC/EB/EI/EE 304 DIGITAL ELECTRONICS (1999 Admissions onwards)

Time: 3 Hours

Max. Marks: 100

(All questions carry **Equal** marks)

- I. (a) Explain the basic principle of Karnaugh map.
(b) Use Karnaugh map to simplify

$$f(ABCD) = \sum_m(1, 3, 4, 7, 11, 13, 15)$$
- OR**
- II. (a) (i) Describe the features of decimal, octal, binary and hexadecimal number systems.
(ii) Explain how a decimal number can be converted into octal, binary and hexadecimal numbers.
(b) Realise the function

$$f = AB + \bar{C}D + \bar{B}$$
using NAND gates only.
- III. (a) With truth tables explain the features of T and D flip-flops.
(b) Explain the operation of a modulo-9 counter.
- OR**
- IV. (a) Draw the circuit diagram and explain the operation of a MOD-12 down counter.
(b) With an example explain the principle of state tables and state diagrams.
- V. (a) Explain the principle of serial and parallel addition in digital circuits.
(b) Draw the circuit of a monostable multivibrator using discrete gates. Explain its operation with relevant waveforms.
- OR**
- VI. (a) Explain 'binary division' in digital circuits.
(b) Draw the circuit diagram of a carry look ahead adder and explain its operation.
- VII. (a) Describe the features of PAL 22 V10.
(b) Compare PAL and PLA.
- OR**
- VIII. (a) Describe the constructional features and operation of semiconductor RAM.
(b) Describe the features and applications of a typical PLA device.
- IX. (a) Sketch the transfer characteristics of TTL inverter. Describe the features of various regions of the characteristics.
(b) Explain how CMOS to TTL interfacing can be done.
- OR**
- X. (a) Describe a circuit arrangement for interfacing TTL to CMOS.
(b) Write notes on :
(i) Standard logic levels.
(ii) Noise margin.

