

B.Tech. Degree III Semester Examination
January 2002

CS/EC/EB/EI/EE 304 - DIGITAL ELECTRONICS

Time: 3 Hours

Maximum Marks: 100

(Answer one question from each module)

(U)

MODULE - I

- I. (a) (i) Convert $(11011.11001)_2$ to Hexadecimal.
(ii) Convert $(321.72)_{10}$ to BCD (8-4-2-1) code and Excess-3 code.
(iii) Convert $(11001)_2$ to Gray code. (8)
- (b) Reduce the function $f(A, B, C, D) = \sum m(0, 7, 8, 9, 10, 12) + \sum d(2, 5, 13)$ using Quine-Mc Cluskey method and implement the function using NAND gates only. (12)
- OR**
- II. (a) A 2 bit binary multiplier accepts two words $A = a_2a_1$ and $B = b_2b_1$, and produces the output $Z = z_3z_2z_1z_0$. Implement the circuit using NAND gates only. (10)
- (b) Write a note on Gray code. Explain why it is called a 'reflective code'. (10)

MODULE - II

- III. (a) Explain 'race around' problem. Explain the ways to circumvent this problem. (8)
- (b) Draw the circuit of a 3-bit universal Shift Register and briefly explain its operation. (12)
- OR**
- IV. (a) Draw the circuit of an asynchronous Decade UP/DOWN counter with mode control input M. (12)
- (b) With a circuit diagram, explain the operation of a 3-bit ring counter. (8)

MODULE - III

- V. (a) Design an astable multivibrator using NAND gates to generate 10 KHz symmetric square wave. Draw relevant waveforms. (10)
- (b) Draw the block diagram of a 4-bit binary divider and explain the operation. (10)
- OR**
- VI. (a) Design a 4-bit binary ripple carry adder using Full Adders. What is the delay involved? (10)
- (b) Implement a Full subtractor using minimum number of NOR gates. (10)

MODULE - IV

- VII. (a) What is an EPROM? Discuss the methods to erase data stored in EPROMs? (6)
- (b) Compare Static RAM and Dynamic RAM. (6)
- (c) Draw the architecture of a 4 x 8 ROM. (8)
- OR**
- VIII. (a) Write a note on Programmable Logic Devices (PLDs). (8)
- (b) Implement the following Boolean functions using PAL.
 $F_1(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13)$
 $F_2(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13, 14)$ (12)

MODULE - V

- IX. (a) Sketch a two input TTL NAND gate circuit. Explain the operation of the circuit. (12)
- (b) Write a short note on ECL. (8)
- OR**
- X. (a) Explain, with neat diagrams, how a CMOS gate can be interfaced with a TTL gate. (10)
- (b) The totem pole output stage of the TTL circuit solved what problem that plagued DTL logic circuits? Explain. (10)

