

B.Tech. Degree III Semester Examination, December 2006

CS/EC/EB/EI/EE 304 DIGITAL ELECTRONICS

(2002 Admission Onwards)

Time: 3 Hours

Maximum Marks: 100

- I. (a) Convert the following from one number system to another number system.
  - (i)  $(237)_1 \rightarrow (x)_{10}$       (ii)  $(CF3D)_{16} \rightarrow (y)_{10}$
  - (iii)  $(.111111)_2 \rightarrow (z)_{10}$       (iv)  $(45.312)_8 \rightarrow (k)_2$
  - (v)  $(1000)_{10} \rightarrow (P)_2$  (10)
- (b) Explain Demorgan's theorem and prove it by using induction method. (5)
- (c) Simplify the following expression by using Boolean laws. (5)

$AB + A\bar{C} + A\bar{B}C (AB + C)$

OR

- II. (a) Simplify the following function by using the Quire Mccleuskey method. (8)  
 $F(w, x, y, z) = \sum m(0, 1, 2, 8, 10, 11, 14, 15)$
- (b) Design a logic circuit using basic logic gates with 4 1/p DCBA that will produce a '1' output only whenever two adjacent input variables are 1's D and A are to be treated as adjacent in this problem. (4)
- (c) Find the reduced SOP form of the following expression (4)  
 $F(w, x, y, z) = \sum m(0, 7, 8, 9, 10, 12) + \sum d(2, 5, 13)$
- (d) What is meant by combinational circuit? How multiplexer is constructed by using the above circuit? (4)
- III. (a) What is meant by Latch and explain different type of Flip-flop used in digital circuits. (10)
- (b) Convert JK Flip-flop to T and D Flip-flop. (5)
- (c) Compare Asynchronous and synchronous counter. (5)

OR

- IV. (a) Explain the different type of shift registers. (6)
- (b) Design mod-5 synchronous counter using JK Flip-flop and implement it. Also draw a timing diagram at the above circuit. (9)
- (c) Explain the different steps required for the design of clocked sequential circuits. (5)
- V. (a) Draw and explain the circuit diagram of full adder using NAND only. (6)
- (b) Compare serial and parallel adder. (4)
- (c) Draw the circuit diagram of a carry look ahead adder and explain its operation. (7)
- (d) Explain the operation of a 4 bit parallel adder-subtractor unit. (3)

OR

- VI. (a) Explain the block diagram of parallel binary multiplier. (7)
- (b) Design and construct Astable Multivibrator using discrete gates. (8)
- (c) Explain four bit Johnson and ring counter using Flip-flop and also draw the tuning diagram. (5)
- VII. (a) Explain the different type of memory in detail. (6)
- (b) Explain the PLA and PAL circuit in detail. (8)
- (c) A combinational circuit is defined by the function.

$F_1 = \sum m(3, 5, 7)$

$F_2 = \sum m(4, 5, 7)$

Implement the circuit with PLA. (6)

OR

- VIII. (a) Write short notes on software tools used in Digital circuits design. (8)
- (b) Design a combinational using a ROM. The circuit accepts 3 bit binary numbers and generates its equivalent Excess-3 code. (6)
- (c) Construct a static and dynamic RAM cells using NMOS. (6)
- IX. (a) Explain the standard two input TTL gate (NAND). (8)
- (b) Explain the term Noise margin and figure of merit in digital IC. (6)
- (c) Compare totem pole and open collector. (6)

OR

- X. (a) Explain Tristate TTL Inverter. (7)
- (b) Explain the interfacing of CMOS to TTL and TTL to CMOS in detail. (6)
- (c) Explain the ECL OR/NOR gate. (7)

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